A SPICE Model for Enhancement- and Depletion-Mode GaAs FET's

S. E. SUSSMAN-FORT, MEMBER, IEEE, JEFFREY C. HANTGAN, MEMBER, IEEE, AND F. L. HUANG, MEMBER, IEEE

Abstract — **An improved model for the GaAs MESFET has been implemented in the source code of the circuit-simulation program SPICE. New features include 1) an accurate model for the Schottky barrier, which allows simulation of both enhancement- and depletion-mode devices; 2) detailed modeling of the nonlinear gate–source and gate–drain capacitances; and 3) a user-specifiable value for the exponent in the expression for the dependence of the dc drain current upon the gate–source voltage. Also discussed are some important points concerning the charge–voltage equations that must accompany the new model's capacitance–voltage equations within SPICE. The new GaAs FET SPICE model is believed to be the most comprehensive one available to date in the public domain.**

I. Introduction

GALLIUM ARSENIDE continues to grow in importance as a material for use in ultra-high-speed digital and analog circuits. The past several years have seen the development of LSI-complexity GaAs digital integrated circuits (IC's) that run at least an order of magnitude faster than comparable silicon circuits at the same power consumption. In analog systems, microwave integrated circuits (MIC's) using GaAs devices and technology have replaced the much bulkier waveguide and traveling-wave tube structures used in avionics and satellite applications.

A necessary part of any IC design is the computer simulation of the circuit in question. The public-domain SPICE [1] program has long been available to designers for the purpose of simulating the time-domain and frequency response behavior of silicon IC's. However, there have been no nonproprietary programs available for accurate GaAs IC simulation.[1] This fact motivated our recent work [2], where we demonstrated, for the first time, a computer model for the depletion-mode GaAs FET which had been installed directly in the source code of SPICE. (See also [3] for another SPICE model of the depletion-mode GaAs FET.) Since the introduction of our model, more than 60 copies of the SPICE modifications needed to include the model have been distributed worldwide by the author. The purpose of this paper is to present an updated version of the GaAs FET SPICE model which now: 1) allows an arbitrary exponent for the dependence of the drain current upon the gate–source voltage; 2) features complete modeling of the Schottky barrier to permit simulation of both enhancement-mode and depletion-mode devices; and 3) contains greatly improved models for the nonlinear gate–source and gate–drain capacitances and instantaneously stored charges. We believe our GaAs FET SPICE model to be the most complete and detailed model available to date in the public domain.

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S. E. Sussman-Fort and J. C. Hantgan are with the Department of Electrical Engineering, State University of New York, Stony Brook, NY 11794.

F. L. Huang is with the Gould Research Center, Rolling Meadows, IL.

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[1] One proprietary SPICE model was recently announced by the Semiconductor Research Cooperative, Research Triangle Park, NC, in their Sept. '85 newsletter.

II. The Updated GaAs MESFET Model

A. The dc Model

The equivalent circuit for the n-channel GaAs FET is a variation of that developed by Curtice [4] and is shown in Fig. 1. The basic dc relationship for the model is

$$I_{ds} = \beta(V_{gs} - V_{to})^n(1 + \lambda V_{ds})\tanh(\alpha V_{ds})$$

where

I_{ds}	drain current,
V_{gs}, V_{ds}	gate–source and drain–source voltage,
β	transconductance parameter,
V_{to}	threshold voltage,
n	exponent factor,
λ	channel length modulation parameter.
α	hyperbolic tangent function parameter.

Referring to Fig. 1, R_d, R_s, and R_g are the resistances of the contact regions; C_{ds} is the (constant) drain–source capacitance; $D1$, $D2$, and R_{ss} form the model for the Schottky barrier; and C_{gs} and C_{gd} are the nonlinear gate–source and gate–drain capacitances. The models for the Schottky barrier, C_{gs}, and C_{gd} are further explained below.

B. The Schottky-Barrier Model

The dc model for the Schottky-barrier diode in Fig. 1 was formulated by Estreich [5] and consists of elements $D1$, $D2$, and R_{ss}. The inclusion of the equivalent circuit for the Schottky barrier in the circuit of Fig. 1 allows accurate simulation of forward bias conditions and consequently permits the modeling of enhancement-mode (as well as depletion-mode) GaAs FETs.

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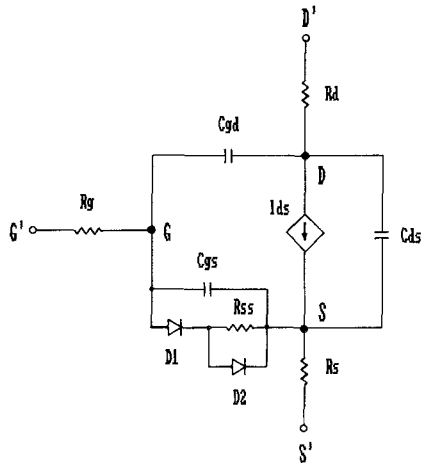

Fig. 1. GaAs FET equivalent circuit.

$D1$ and $D2$ are described by the standard dc p n junction diode equations contained within SPICE. The parameters that need to be specified for these diodes are as follows:

for $D1$

N_p	emission coefficient
I_s	saturation current

for $D2$

N_s	emission coefficient
I_{ss}	saturation current.

To accurately model the Schottky spreading, bulk and ohmic resistances, R_{ss} and the bulk resistance of diode $D1$ must also be included as parameters of the complete Schottky-diode model. In our implementation, we use R_g to represent the bulk resistance of diode $D1$. Hence, R_g is seen to serve a dual purpose, since it also models the resistance of the gate contact region, as mentioned previously. Reference [5] gives typical values for these parameters, and also explains a method for obtaining the parameter values from experimental data.

C. The Nonlinear Gate–Source/Gate–Drain Capacitance Models

The equations for C_{gs} and C_{gd} were derived by Takada *et al.* [6]. These equations, in a slightly modified form, were installed by us in the source code of SPICE. The differences amount to a notation which depends less upon the process parameters and more upon normalized capacitance values. There is no loss of generality in our implementation; in fact, we introduce some additional flexibility by optionally allowing the values for C_{gd} and C_{gs} to be constant—rather than voltage-dependent—if so desired.

In the equations for C_{gs} that follow, V_{to} is the threshold voltage, $V_a = V_{to} - 0.15$, $V_b = V_{to} + 0.08$, V_{bi} is the built-in voltage, $CGS0$ is the zero-bias gate–source capacitance, and FC is the product of the GaAs permittivity with the gate width (i.e., the ϵW factor in [6]).

$V_{gs} < V_a$:

$$C_{gs} = FC \arctan\sqrt{(V_{bi} - V_{to})/(V_{to} - V_{gs})}.$$

$V_a < V_{gs} < V_b$:

$$C_{gs} = \left[(V_{gs} - V_a)/0.23\right] \cdot \left[CGS0/\sqrt{(1 - V_b/V_{bi})} + \pi FC/2 - FC \arctan\sqrt{(V_{bi} - V_{to})/0.15}\right] + FC \arctan\sqrt{(V_{bi} - V_{to})/0.15}.$$

$V_{gs} > V_b$:

$$C_{gs} = CGS0/\sqrt{(1 - V_{gs}/V_{bi})} + \pi FC/2.$$

The equations for C_{gd} are exactly the same except that CGD, the zero-bias gate–drain capacitance, is to be substituted for $CGS0$ and that V_{gd}, the gate–source voltage, is to be substituted for V_{gs}.

It should be noted that FC appears in the sets of equations for both C_{gs} and C_{gd} and that a single specification for FC completely defines the contribution from this parameter. However, we have arranged the SPICE source code so that whenever CGD is set equal to zero, FC will also be treated as zero insofar as the expressions for C_{gd} are concerned. FC will continue, however, to contribute its actual specified value to the equations for C_{gs}. In an entirely similar manner, whenever $CGS0$ is set equal to zero, FC will contribute to the expressions for C_{gd} only.

We have included a mechanism within our GaAs FET SPICE model implementation to completely bypass the above equations for C_{gs} and/or C_{gd} and then to treat these capacitances as constant (rather than voltage-dependent) values. One need only specify $CGS0$ and/or CGD as a *negative* value in the SPICE data file. The program will then set $C_{gs} = |CGS0|$ and/or $C_{gd} = |CGD|$ (regardless of the value given for FC).

D. The Charge–Voltage Equations for C_{gs} and C_{gd}

In [6], Takada *et al.* derived the capacitance equations for the GaAs FET by first developing the charge–voltage ($Q-V$) equations for the device and then differentiating these expressions with respect to voltage. Takada's $Q-V$ relations can be thought of as including contributions from both the static charge distribution and the excess charge arising from applied voltages. The static charge is a function of the device geometry and processing only (i.e., not a function of applied voltage) and hence does not contribute to the $C-V$ equations.

SPICE 2G.5 needs both $Q-V$ and capacitance–voltage ($C-V$) equations for its voltage-dependent capacitance models. However, the $Q-V$ equations that SPICE requires are those *only* for the excess charge transferred within the device due to the application of external voltages. Hence, there is a difference between the Takada $Q-V$ equations and the $Q-V$ equations that SPICE requires.

Fortunately, this difference is easily resolved. One need only recognize that SPICE's $Q-V$ equations must satisfy

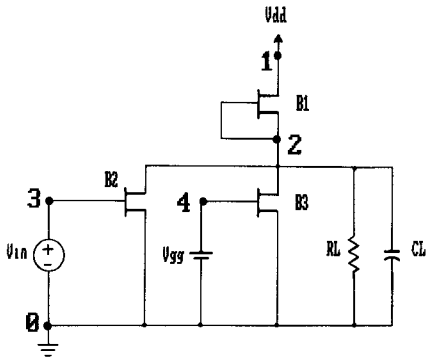

Fig. 2. Two-input NOR gate.

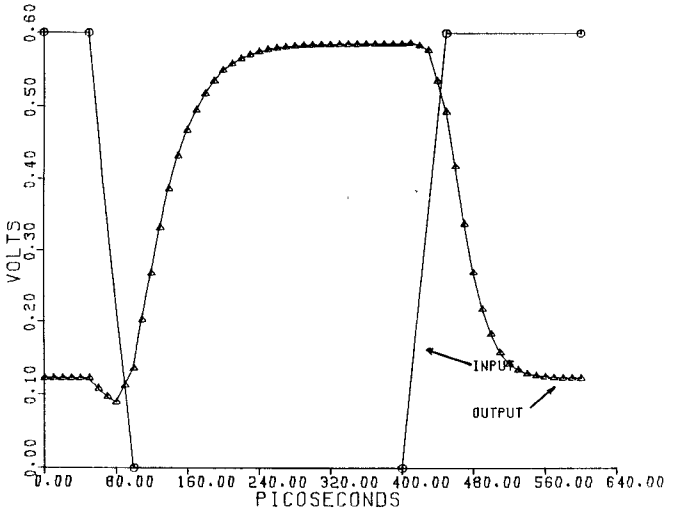

Fig. 3. Transient response of two-input NOR gate.

zero initial energy storage; namely, if $Q = f(V)$, then $f(0)$ must be zero. To develop the SPICE $Q-V$ equations, the procedure is simply to add a constant to each of the Takada $Q-V$ equations defined for the various ranges of V_{gs}. The constants are evaluated by requiring the charge at $V_{gs} = 0$ to be zero and by enforcing continuity of charge at the boundaries of the regions defined for V_{gs}. The process is complicated somewhat by the fact that the transition region defined by Takada

$$V_{gs} \in [V_{to} - 0.15, V_{to} + 0.08]$$

may be wholly positive, wholly negative, or partially positive and negative. The solution to this difficulty is to derive three sets of constants for the various cases. We have included in SPICE the appropriate $Q-V$ equations which properly model the excess charge stored in a GaAs FET for the various ranges of V_{gs} and values of V_{to}. The complete set of charge–voltage equations for SPICE is given in subroutine GASFET, which will be made available to interested readers (see Section IV).

It is significant to point out that during a transient analysis, SPICE 2G.5 does solve for the instantaneous charge stored in the capacitors of the circuit in question. This is part of the "companion modeling" [7] process, whereby the task of numerically solving the nonlinear differential equations of the circuit is performed by repetitively analyzing a continually updated linear circuit—the companion model—at a sequence of discrete time points. However, the solution for the charge is not available to the user, and is usually of no interest anyway. More importantly, solving for the charge adds to the problem complexity and can cause SPICE to fail to converge to a solution, especially if the $Q-V$ equations are not derived carefully.

It is possible to perform the transient analysis of a circuit on a computer without resorting to solving explicitly for capacitor charge (or inductor flux, for that matter). Such a method is discussed in [8], where a simplified companion model for the nonlinear capacitor is developed which depends only upon the element voltage and the *derivative* of charge with respect to voltage at a given time step. It is our intuitive feeling—one which we hope to confirm with future numerical experiments—that this method of nonlinear circuit analysis has better convergence properties than the one which requires explicitly solving for charge.

III. An Example

The example considered is a two-input NOR gate consisting of a depletion-mode GaAs FET pull-up device, and two enhancement-mode GaAs FET pull-down devices, as shown in Fig. 2. The circuit output is loaded by an RC network, and the gate of one of the enhancement-mode devices is set just at its threshold voltage. Under these conditions, the response of the circuit to a trapezoidal input pulse was calculated by SPICE. A plot of the results is shown in Fig. 3.

The SPICE data file for the transient analysis is given in Appendix I. The data for the example were supplied in part by J. Irvine [9]; the parameters for the Schottky-diode modeling were extrapolated from the data of [5].

The complete user's guide for the GaAs FET model, which shows all specifiable parameters and default values, is given in Appendix II.

IV. Conclusions

A new SPICE model for enhancement- and depletion-mode GaAs FET's has been developed. The model offers capabilities not previously available in public-domain software. Interested readers should contact the second-named author concerning arrangements for distributing the modified SPICE source code. The present modifications, which involve changes to 17 subroutines, are applicable to SPICE version 2G.5; the modifications pertinent to version 2G.6 are expected to be available in the near future.

Appendix I.
SPICE Data File for the Example of Fig. 2

Two-Input GaAs FET NOR Gate

```
*
* Depletion-Mode Device: MESFET 1UM, 20
  UM VT=-0.5V
```

```
* Enhancement-Mode Device: MESFET 1UM,
  50UM VT=+0.1V
VDD 1 0 0.6 DC
VIN 3 0 PULSE (0.6 0.01 50P 50P 50P 300P
  700P)
RLOAD 2 0 20K
B1 1 2 2 DFET
B2 2 3 0 EFET
B3 2 4 0 ENFET
VGG 4 0 0.1 DC
CL 2 0 .06PF
*
* Depletion-Mode
.MODEL DFET GASFET(Vto=-.5, Beta=.00214,
  Rd=125, Rs=125, CGS0=.028PF,
+ CGD=.004PF, Lambda=.483, Vbi=.74, Alpha=
  6.725, FC=0.001PF, Sqrlaw=1.92)
*
* Enhancement-Mode
.MODEL EFET GASFET(Vto=.1, Beta=.0090, Rd=
  50, Rs=50, CGS0=.070PF,
+ CGD=.010PF, Alpha=4.9, Vbi=0.74, Is=25E-
  14, Rss=90, RG=70,
+ Np=1.1, Ns=.389, Iss=14.4E-6, FC=
  0.001PF)
*
* Enhancement-Mode
.MODEL ENFET GASFET(Vto=.1, Beta=.0090, Rd
  =50, Rs=50,
+ Alpha=4.9, Vbi=0.74, Is=25E-14, Rss=90,
  RG=70,
+ Np=1.1, Ns=.389, Iss=14.4E-6,
+ CGS0=0.070PF, Tau=7PS)
*
 .TRAN 10P 1.0N
 .PRINT TRAN V(3) V(2)
 .PLOT TRAN V(3) V(2)
 .END
```

APPENDIX II.
USER'S GUIDE FOR THE GAAS FET SPICE MODEL

Model usage

Bxxx Drain_Node_Number Gate_Node_Number Source_Node_Number Your_Model_Name
.MODEL Your_Model_Name GASFET(parameter1 = value1, parameter2 = value2,...)

Example

B7 1 3 5 ENHANCE
.MODEL ENHANCE GASFET(Vto = 0.1, Alpha = 1.9, CGS0 = 0.002PF, Sqrlaw = 2.07)

Parameter Variable	Parameter Description	Default Value
V_{to}	Threshold voltage	−2.5 V
V_{bi}	Built-in voltage	1.0 V
R_g	Gate resistance	0.0 Ω
R_d	Drain resistance	0.0 Ω
R_s	Source resistance	0.0 Ω
alpha	Hyperbolic tangent parameter	2.0/V
beta	Transconductance parameter	1.0e-4 A/V**2
lambda	Channel length modulation factor	0.0
$CGS0$	Zero-bias gate–source capacitance	0.0 F
CGD	Zero-bias gate–drain capacitance	0.0 F
FC	Permittivity width product	0.0 F
C_{ds}	Drain–source capacitance	0.0 F
I_s	Saturation current for diode $D1$	1.0E-14 A
N_p	Emission coefficient for diode $D1$	1.0
I_{ss}	Saturation current for diode $D2$	1.0E-14 A
N_s	Emission coefficient for diode $D2$	1.0
R_{ss}	Resistor in parallel with diode $D2$	0.0 Ω
tau	Transit time	0.0 sec
SqrLaw	Exponent n in $I_{ds}(V_{gs}, V_{ds})$ equation	2.0

Notes
1) R_g is also used as part of the Schottky-diode model.
2) If $R_{ss} = 0$, then the Schottky-diode model reduces to diode $D1$ alone.
3) Parameter values not specified in the .Model statement assume the default values given above.

REFERENCES

[1] L. W. Nagel, "SPICE2: A computer program to simulate semiconductor circuits," Electron. Res. Lab., Univ. California, Berkeley, Memo ERL-M520, 1975.

[2] S. E. Sussman-Fort, "A complete GaAs MESFET computer model for SPICE," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-32, pp. 471–473, Apr. 1984.

[3] J. M. Goglio, J. R. Hauser, and P. A. Blakey, "A large-signal GaAs MESFET model implemented on SPICE," *IEEE Circuits and Devices Magazine*, vol. 1, no. 5, pp. 21–30, Sept. 1985.

[4] W. R. Curtice, "A MESFET model for use in the design of GaAs integrated circuits," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-28, pp. 448–456, May 1980.

[5] D. B. Estreich, "A simulation model for Schottky diodes in GaAs integrated circuits," *IEEE Trans. Computer-Aided Design*, vol. CAD-2, no. 2, pp. 106–111, Apr. 1983.

[6] T. Takada, K. Yokoyama, M. Ida, and T. Sudo, "A MESFET variable capacitance model for GaAs integrated circuit simulation," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-30, pp. 719–723, May 1982.

[7] D. A. Calahan, *Computer-Aided Network Design*. New York: McGraw-Hill, 1972, ch. 4.

[8] L. O. Chua and P. M. Lin, *Computer-Aided Analysis of Electronic Circuits: Algorithms and Computational Techniques*. Englewood Cliffs, NJ: Prentice-Hall, 1975, ch. 17.

[9] ITT Defense Communications Division, Nutley, NJ, private communication.

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S. E. Sussman-Fort (S'75–M'78) received the B.E.E. degree from the City College of the City University of New York in 1969, the M.S.E. degree from Princeton University in 1971, and the Ph.D. degree from the University of California, Los Angeles, in 1978.

From 1969 to 1973, he was employed by Bell Laboratories, Holmdel, NJ, where he was engaged in the design of RC, thin-film active filters. During 1974, he was with the Burroughs Corporation, Pasadena, CA, where he developed current-mode logic circuits. During his doctoral studies at UCLA from 1974 to 1978, he had summer and part-time jobs at the TRW Systems Group, the Aerospace Corporation, and the Torrance Research Center of Hughes Aircraft Company, where he was involved in the analysis and design of frequency synthesizers, microwave filters, and microwave GaAs FET circuits. He was on the faculty of North Carolina State A&T State

University, Greensboro, NC during 1978–79 and was with Rensselaer Polytechnic Institute, Troy, NY, during 1979–80. During the summer of 1979, he was with the IBM Corporation, Research Triangle Park, NC, where he developed computer models of radio anechoic chambers. In 1980, he joined the Electrical Engineering Department of the State University of New York at Stony Brook, where he is now Associate Professor and Director of both the VLSI and CAD Research Laboratories. Since 1979, he has served as a consultant in electronics and computer-aided design to several industrial firms. In addition, he is presently an Associate Editor of the IEEE CIRCUITS AND SYSTEMS MAGAZINE. Dr. Sussman-Fort's research interests encompass the areas of VLSI-CAD, network theory, and microwave circuits.

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Jeffrey C. Hantgan (S'75–M'79) received the B.S.E.E. degree with Special Honors from The George Washington University, Washington, DC, in 1973 and the M.S. and Ph.D. degrees from Cornell University, Ithaca, NY, in 1977 and 1981, respectively.

In 1981, he joined the faculty of the State University of New York at Stony Brook, where he is an Assistant Professor in the Department of Electrical Engineering. His current research is in the areas of surface wave mode modeling in open dielectric waveguides at microwave and optical frequencies, and the enhancement of general circuit simulation programs such as SPICE to include additional and/or improved device models.

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F. L. Huang (S'84–M'85) photograph and biography unavailable at the time of publication.